Form PTO-1449 U.S. Dept. of Commerce Patent & Trademark Office List of Documents Cit d by Applicant (Use several sheets if necessary)	Atty. Docket: 00-LM-134	Serial No. 10/033,992
	Applicant: William A. CHREN, Jr.	
	Filing Date: December 27, 2001	Group: 2121

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Ex'rs In'		Document Number	Date	Name	Class	Sub-class	Filing Date, if applicable
	AA1	5,892,632	April 6, 1999	Behrens et al.			
	AA2	09/383,478					August 26, 1999
	AA3	09/656,550					September 6, 2000

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	AA4	Chren, W.A. Jr., "One-Hot Residue Coding for Low Delay-Power Product CMOS Design", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, v. 45. no. 3, March 1998, pgs. 303-313.
	AA5	Karim Arabi et al., "Oscillation Built-In Self-Test (OBIST) Scheme for Functional and Structural Testing of Analog and Mixed-Signal Integrated Circuits", Proceedings of the IEEE International Test Conference, Washington, D.C., 1997, pp. 786-795.
	AA6	N. S. Szabo, et al., "Residue Arithmetic and its Applications to Computer Technology, McGraw-Hill, 1967, pgs. 147-150.
	AA7	Chren, W.A. Jr., "A New Residue Number System Division Algorithm", Computers and Mathematics with Applications, vol. 19, no. 7, 1990, pgs. 13-29, 1990.
	AA8	Gago, A. et al. "Reduced Implementation of D-Type DET Flip-Flops", IEEE Journal of Solid-State Circuits, Vol. 28, No. 3, March 1993, pp. 400-402.
	AA9	Farrahi, A. et al. "Activity-Driven Clock Design", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 6, June 2001, pp. 705-714.
	AB1	Rabaey, J.M. "Digital Integrated Circuits: A Design Perspective", Prentice Hall, 1996, pp. 528-530.

Examiner: D. H. Malzahn	Date Considered: 9/30/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.